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ABSTRACT

The design of β-Ga_2O_3-based modulation-doped field effect transistors is discussed with a focus on the role of self-heating and resultant modification of the electron mobility profile. Temperature- and doping-dependent model of the electron mobility as well as temperature- and orientation-dependent approximations of the thermal conductivity of β-Ga_2O_3 are presented. A decrease in drain current was attributed to a position-dependent mobility reduction caused by a coupled self-heating mechanism and a high electric-field mobility reduction mechanism. A simple thermal management solution is presented where heat is extracted through the source contact metal. Additionally, it is shown that an undesired secondary channel can form at the modulation-doped layer that is distinguished by an inflection in the transconductance curve.

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I. INTRODUCTION

Monoclinic β-Ga_2O_3-based transistors possess fundamental electronic properties that are advantageous for high power devices.[1] A number of these properties derive directly from the wide bandgap of β-Ga_2O_3 ($E_g = 4.8$ eV) including an exceptionally high electric breakdown field (approximately 8 MV/cm).[2] The high breakdown field allows for the design of a lateral transistor with a short channel that can withstand a high critical field. The short channel design lowers the switching loss and, also, lowers the on-resistance, which reduces the conduction loss.[3] Additionally, the short channel allows the high-voltage switch to operate at high frequency (>1 MHz) and, thus, enables a system design with smaller (size and weight) passive circuit components.[4]

A lateral metal-semiconductor or metal-oxide-semiconductor field effect transistor is typically based on an n-type doped channel. At carrier concentrations greater than 1×10^{18} cm^{-3}, the mobility of β-Ga_2O_3 is limited to approximately 50 cm^2/V s due to impurity scattering.[5] In contrast, at a carrier concentration of 2.5×10^{16} cm^{-3}, a mobility of β-Ga_2O_3 of 184 cm^2/V s has been reported—primarily limited by polar optical phonon scattering.[6] This provides the motivation for a modulation-doped design where donors within the $(Al_xGa_{1-x})_2O_3$ barrier accumulate in a triangular potential well in the undoped Ga_2O_3 crystal at the $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ interface. An $(Al_xGa_{1x})_2O_3$ spacer layer physically separates the dopant atoms from the electrons in the conductive channel, which reduces impurity scattering and, thus, improves electron mobility.

With proper design, conduction predominantly occurs via the dense two-dimensional electron gas (2DEG) that forms in the potential well. Nevertheless, a deleterious secondary channel may form at the modulation-doping location in the $(Al_xGa_{1x})_2O_3$ barrier. See supplementary material[23] for general design rules for an optimal formation of the 2DEG. The supplementary material[23] focuses on mitigating three limitations related to current deposition technology involving the aluminum content in $(Al_xGa_{1-x})_2O_3$, modulation-doping concentration, and the persistent tail of dopant atoms. Below, it is shown that residual charge in the $(Al_xGa_{1-x})_2O_3$ barrier manifests as a secondary inflection in the transconductance curve.

This primary aim of this article is to investigate the coupled relation of on-state self-heating and spatially dependent mobility reduction, and the resultant alteration of the forward bias response.

The mobility decreases significantly at elevated temperature and the low thermal conductivity of β-Ga_2O_3 results in self-heating of the device at moderate current density. Approximations to the mobility and thermal conductivity of β-Ga_2O_3 are presented that can be readily implemented in a Technology Computer-Aided Design (TCAD) simulation environment. It is shown that self-heating and the electric-field dependence will significantly alter the cross-sectional mobility profile. Significant self-heating can result in a negative differential conductance in the drain current response to increasing drain voltage.

II. MODELING

A series of electrothermal simulations, via the Silvaco TCAD environment, were conducted for a modulation-doped $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ structure to provide insight into the device current-voltage relationships as well as the cross-sectional profiles of current density, mobility, and temperature.

A. Thermal conductivity and mobility models

An accurate description of the temperature dependent parameters is necessary for the simulation of a transistor based on Ga_2O_3, which suffers from self-heating related to its low thermal conductivity. For application to a TCAD simulation, the thermal conductivity model given in Mu *et al.*[7] was fit to a power-law thermal model given by

$$\kappa(T) = \kappa_{300}\left(\frac{T}{300}\right)^{\alpha}, \tag{1}$$

with the parameters listed in Table I.

Ma *et al.* developed a model of mobility of Ga_2O_3 that accounted for several scattering mechanisms.[8] The Ma mobility model, based on the Boltzmann transport equation via the relaxation-time approximation solution, requires two separate integrations. To introduce a temperature and donor dependent model into the device simulation, the Boltzmann model of Ma *et al.* was fit to the Arora low-field mobility model[9] with a structure in the Silvaco TCAD environment given by

$$\mu_n = \mu_1\left(\frac{T}{300}\right)^{\alpha} + \frac{\mu_2\left(\frac{T}{300}\right)^{\beta}}{1 + \frac{N}{N_{crit}\left(\frac{T}{300}\right)^{\gamma}}}, \tag{2}$$

with fitting parameters given by $\mu_1 = 1.679\,38\ \mathrm{cm^2/V\,s}$, $\mu_2 = 264.557\ \mathrm{cm^2/V\,s}$, $\alpha = -0.116\,259$, $\beta = -2.292\,57$, $\gamma = 2.644\,26$, and $N_{crit} = 4.294\,47 \times 10^{18}\ \mathrm{cm^{-3}}$.

Figure 1(a) displays the calculated mobility of the Arora model compared to the calculated Ma model and the specific scattering mechanisms defined in the Ma model. Figures 1(b) and 1(c) display the Arora calculated mobility as a function of dopant density and temperature. The Arora model replicates the Ma model, which predicts a transition from polar optical phonon scattering as the limiting mechanism at a low donor level to impurity scattering as the dominant mechanism limiting the mobility, above 200 °K, at a high donor level.

TABLE I. Orientation-dependent model parameters for thermal conductivity for Ga_2O_3 and $AlGaO_3$, and a heatsink material comparable to ceramic poly-AlN.

		κ_{300} (W/cm K)	α
Ga_2O_3	[100]	0.111	−1.334 87
	[010]	0.155	−1.255 26
	[001]	0.153	−1.312 47
$AlGaO_3$	[100]	0.198	−1.623 31
	[010]	0.25	−1.485 43
	[001]	0.304	−1.613 16
Heat sink		1.8	−1.3

B. Device structure

The base simulation structure consists of 20 nm Atomic Layer Deposition (ALD) Al_2O_3, 30 nm $(Al_{0.25}Ga_{0.75})_2O_3$ with a background donor concentration of $1 \times 10^{17}\ \mathrm{cm^{-3}}$ and modulation doped at $4 \times 10^{19}\ \mathrm{cm^{-3}}$ with a Gaussian distribution with a characteristic length of 0.5 nm that peaks at 4 nm from the layer bottom, 200 nm Ga_2O_3 with a background donor concentration of $1 \times 10^{15}\ \mathrm{cm^{-3}}$, and a 200 μm $(\bar{2}01)$ Ga_2O_3:Fe substrate with a thermal boundary resistance of $0.001\ \mathrm{cm^2\,K/W}$. The source and drain contacts are 50 μm in length and composed of 20 nm Ti and 300 nm Au. The gate contact is 5 μm in length and composed of 20 nm Ni and 300 nm Au. The source to gate spacing is 3 μm and the gate to drain spacing is 12 μm. The remaining structure consists of Si_3N_4.

As shown in Fig. 2(a) heatsink, with a temperature dependent thermal conductivity similar to ceramic poly-AlN, is optionally added. The heatsink is 50 μm in length and ends 5 μm from the edge of the source metal. The heatsink is separated by 50 nm of Si_3N_4 from the source metal. The heatsink has a thermal boundary resistance of $0.001\ \mathrm{cm^2\,K/W}$ and the Ga_2O_3:Fe substrate is thermally isolated.

III. RESULTS

A. Electrothermal simulation with thermal contact to substrate base

A simulation of the device structure was conducted, with a thermal contact to the substrate base, as described in Sec. II. The drain current and the peak temperature as a function of forward drain bias are displayed in Fig. 3(a). At a drain bias above 3 V, the temperature of the device rapidly increases. Additionally, above 7 V, a negative differential conductivity is observed. The increase in temperature relative to the increase in power corresponds to a device thermal resistance ($R_{th} = \Delta T/P_D$) of 167 mm K°/W at 10 V (and 359 °K).

Figure 3(b) displays the drain current and peak temperature as a function of gate bias for a drain voltage of 5 and 10 V. At a drain voltage of 5 and 10 V, the peak device temperature plateaus at approximately 325 and 385 °K, respectively. At a large positive gate

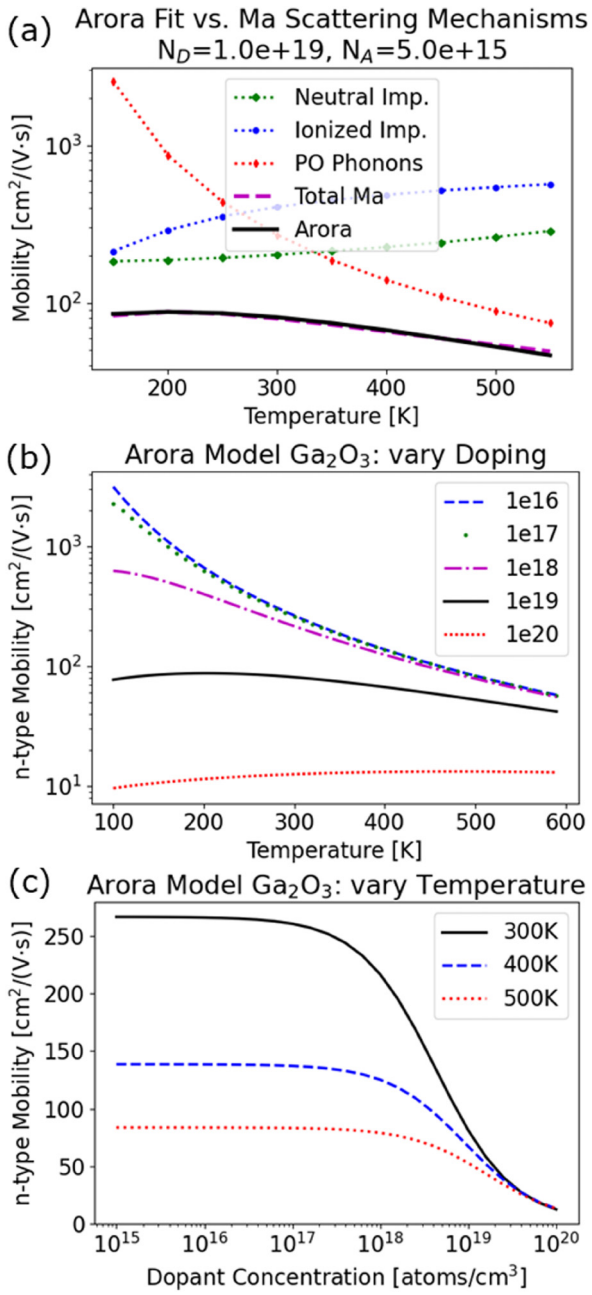

FIG. 1. (a) Comparison of fitted Arora model to Ma mobility model with its relevant scattering mechanisms. Mobility of β-Ga_2O_3 in the Arora model as a function of (b) temperature and (c) donor concentration.

bias, the gate minimally impacts the channel, which behaves similar to a resistor. Moving from a drain voltage of 5–10 V corresponds to a 47% increase in drain current but a 132% increase in temperature.

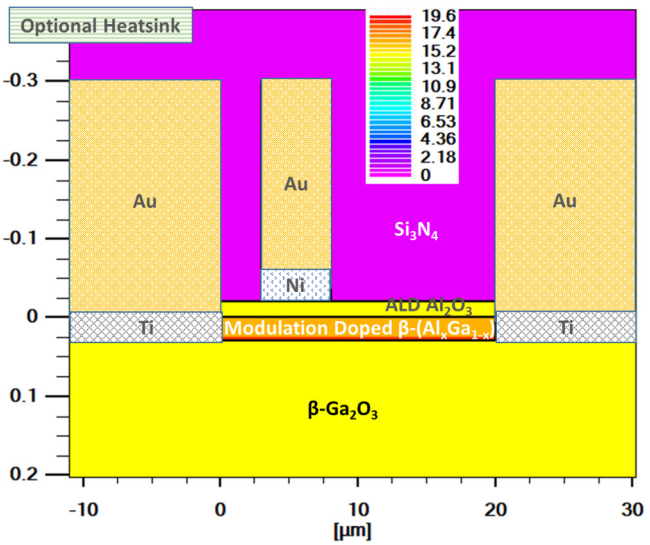

FIG. 2. Components and log donor concentration (cm^{-3}) profile of base simulation structure. The MODFET is designed to have the primary path of current flow in the triangular potential well formed in the first few nanometers in the undoped Ga_2O_3 layer below the $(Al_{0.25}Ga_{0.75})_2O_3/Ga_2O_3$ interface.

Figure 4 compares the log current density, x-component (direction from source to drain) of the mobility, and temperature at a fixed drain current (of $V_d = 10$ V). The left-column corresponds to the near complete depletion of the channel (at $V_g = -4$ V), center-column corresponds to the point of initial depletion (starting at the drain side of the gate edge) in the channel (at $V_g = 0$ V), and right-column is the transitional point of depletion of the $(Al_{0.25}Ga_{0.75})_2O_3$ barrier (at $V_g = 2$ V) in Fig. 4.

In Figs. 4(d) and 4(e), the reduction in mobility at the drain side of the gate edge is caused by the peak in x-component of the electric field as predicted by the high-field dependent mobility model. This causes a local increase in resistance, which similarly causes an increase in Joule heating and a corresponding peak in temperature at the drain side of the gate edge. In Fig. 4(a) (at $V_g = -4$ V), it is seen that the total current is low; thus, the Joule heating throughout the channel is low and the overall temperature increase in the structure is minimal as observable in Fig. 4(g).

In contrast, in Fig. 4(b) (at $V_g = 0$ V), a significant current is flowing in the channel, which causes Joule heating along the length of the channel as well as a relatively higher increase in heating at the drain edge of the gate (due to the high electric-field induced mobility reduction). This generated heat sharply increases the temperature at the drain side of the gate edge in the channel [Fig. 4(h)]. A temperature gradient exists moving away from the gate edge but the temperature in the surrounding structure is sufficient to cause an appreciable reduction in the mobility in the corresponding region [Fig. 4(e)].

The transitional point of depletion of the $(Al_{0.25}Ga_{0.75})_2O_3$ barrier (at $V_g = 2$ V) reveals a small yet discernable secondary current flow in $(Al_{0.25}Ga_{0.75})_2O_3$ barrier near the location of the modulation doping [Fig. 4(c)]. Additionally, at this gate bias,

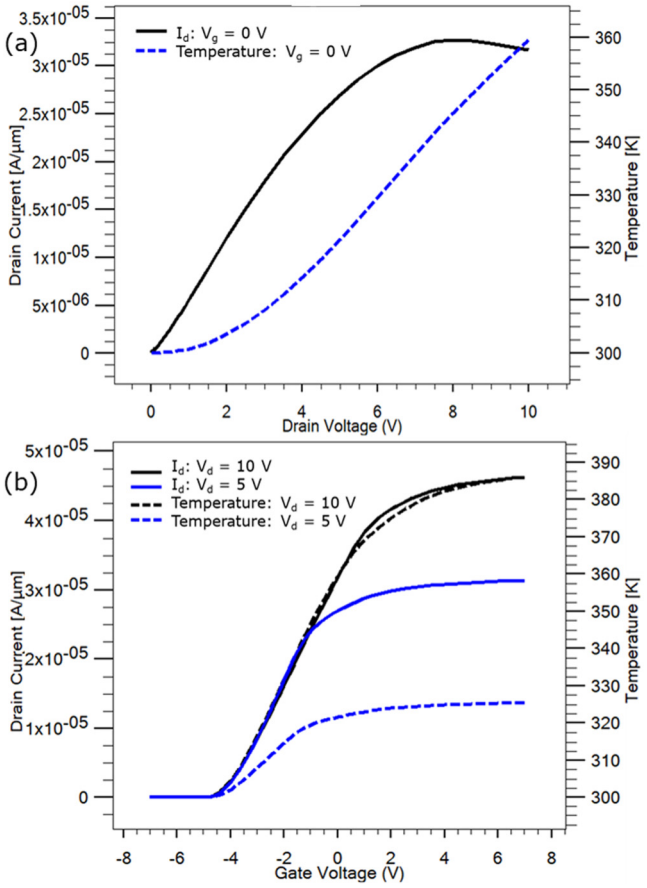

FIG. 3. Drain current and peak temperature as a function of (a) drain voltage at zero gate bias and (b) gate bias at a drain voltage of 5 and 10 V. The temperature vs drain bias in (a) displays a slope of 8.2 K°/V for V_d greater than 5 V.

the electric field from the gate has essential no interaction with the primary channel. Hence, the potential well below the $(Al_{0.25}Ga_{0.75})_2O_3/Ga_2O_3$ interface effectively acts as a high-conductivity resistor. The manifests as heating along the entire channel that creates a non-localized heating profile [Fig. 4(i)] and a relatively uniform reduction in mobility in the Ga_2O_3 [Fig. 4(f)].

B. Comparison to isothermal simulation

A simulation was conducted of the same device structure except thermal heating is neglected, that is, the device is held at 300 °K. Examination of the mobility cross section, in Fig. 5(b), reveals a sharp decrease in mobility at the drain side of the gate edge—and a smaller decrease at the edge of the source contacts. This decrease in mobility is due to the local peak in the electric field. Overall, the isothermal device has a high mobility along the channel, which corresponds to high current density in Fig. 5(a) as compared to the electrothermal simulation in Fig. 4(b).

Figure 6 provides a comparison of the electrothermal simulations to the equivalent isothermal simulations where the lattice temperature is fixed at 300 °K. The drain current at a drain voltage less than 3 V is similar in the thermal and isothermal simulations. This indicates that current density is sufficiently low such that the Joule heat generated can be effectively conducted to and dissipated at the base of the substrate. Additionally, although self-heating is minimal, it is clear the drain voltage is shifting the onset of saturation in drain current—for this particular device geometry and structure.

The drain current and transconductance at a drain voltage of 5 V show a small deviation in the thermal and isothermal simulations for a gate bias greater than −1 V. At this transition point, the current density is sufficiently high that most but not all the Joule heat generated can be effectively dissipated at the base of the substrate. For a drain voltage of 5 V, an inflection is present in the transconductance curve [Fig. 6(b)] at a gate bias of 1 V for both the thermal and isothermal simulation. This inflection corresponds to the point where the gate voltage is sufficiently positive such that the charge, located at modulation-doping position in the $(Al_{0.25}Ga_{0.75})_2O_3$ barrier, is no longer depleted. For a drain voltage of 10 V, a similar inflection is present in the transconductance curve [Fig. 6(b)] at a gate bias of 2 V.

As discussed in Sec. II, at a drain voltage of 10 V, self-heating can raise the temperature of the lattice, which significantly decreases the electron mobility in and near the channel. This increases the resistance of the device, which is evident in the large difference in the thermal and isothermal simulations in Fig. 6.

Figure 6(a) shows a negative differential conductivity for a drain voltage above 7 V with a gate bias of −2 and 0 V. For this particular device structure, negative differential conductivity is not seen for the isothermal simulations. Here, two coupled mechanisms contribute to the negative differential conductivity; specifically, the sharp reduction in mobility at the drain side of the gate edge caused by the peak in the electric field, and the overall reduction in mobility along the entire length of the channel caused by the temperature rise related to self-heating.

C. Heat removal through the source metal

A simple improvement to the thermal design is to place a heatsink material on the surface of the structure near but offset from the source metal. Most transistor test structures have a large source pad above the source region; that is, the source contact is not accessed via a metal finger. As described above, the device surface is covered with an Si_3N_4 layer. A 50 nm Si_3N_4 layer is between the top of the source metal and the heatsink material, and the heatsink material is offset 5 μm from the edge of the source contact. To further simplify the analysis, no heat exits the bottom of the substrate.

Figure 7(a) shows that the drain current saturates at a drain bias greater than 7 V although a slight negative differential conductivity is evident at a drain bias of 10 V. Examination of the temperature cross section, in Fig. 7(b) reveals the expected peak at the drain side of the gate edge—and an overall gradient towards the heat sink located near the source contacts. The increase in temperature relative to the increase in power corresponds to a thermal

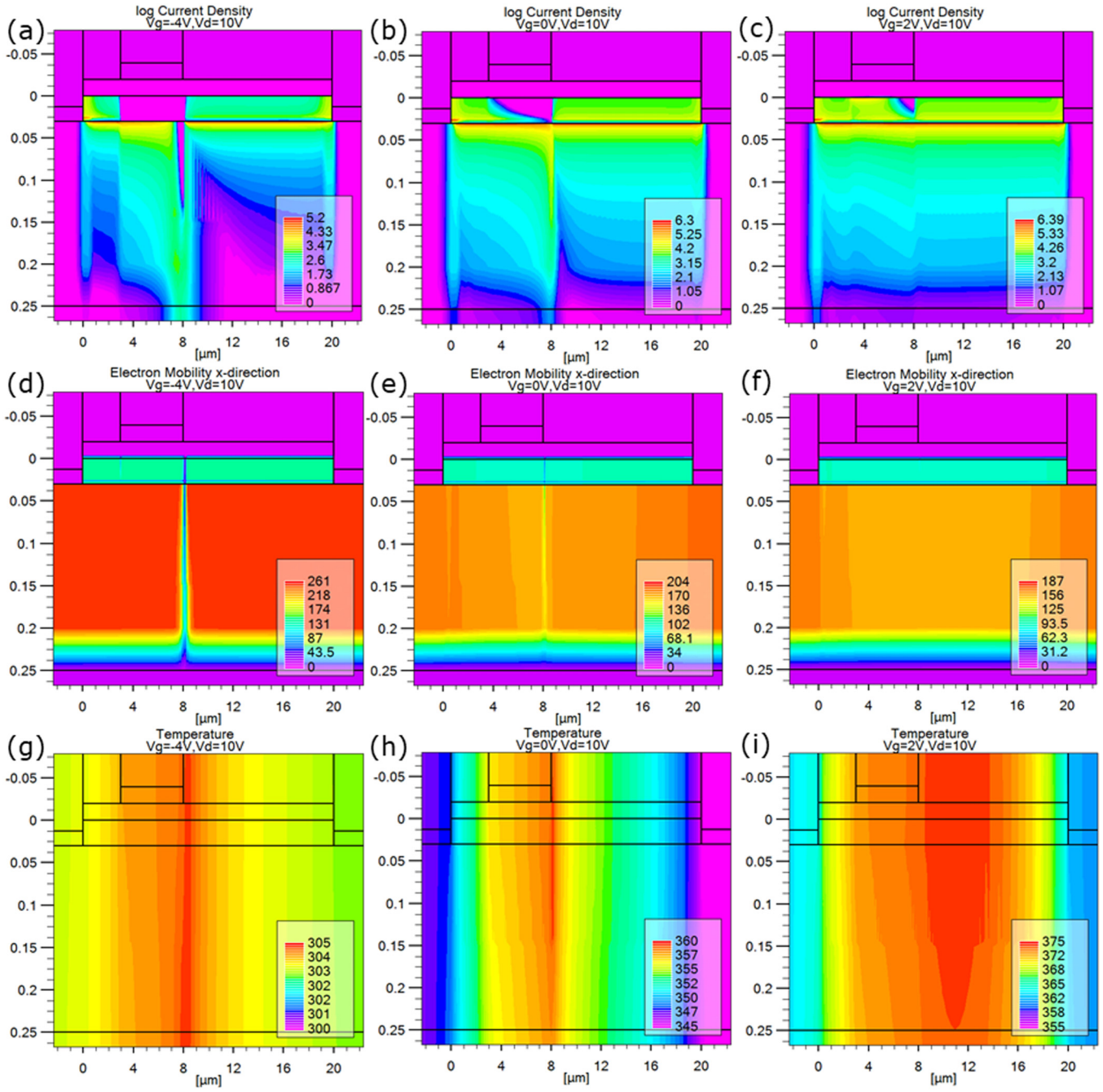

FIG. 4. Cross sections with V_d at 10 V and with V_g at −4 V [(a), (d), and (g)], with V_g at 0 V [(b), (e), and (h)], and with V_g at 2 V [(c), (f), and (i)] for [(a)–(c)] log current density (A/cm^2), [(d)–(f)] x-component of electron mobility (cm^2/V s), and [(g)–(i)] lattice temperature (°K). The left-column corresponds to the near complete depletion of the channel (at $V_g = -4$ V), which greatly reduces (a) current flow; a high electric field reduces the (d) mobility at the gate edge; however, the overall current flow is low, which limits Joule heating. The center-column corresponds to the point of initial depletion (starting at the drain side of the gate edge) of the channel (at $V_g = 0$ V) with (b) significant current flowing along the channel; (e) the sharp reduction in mobility at the drain side of the gate edge is caused by the peak in electric field and the coupled self-heating effect on (h) temperature. The right-column corresponds to the transitional point of depletion of the $(Al_{0.25}Ga_{0.75})_2O_3$ barrier (at $V_g = 2$ V) with (c) large current flowing through the channel with little interaction with the electric field from the gate; (i) a broad heating and temperature profile occurs owing to a relatively uniform Joule heating along the length of the channel.

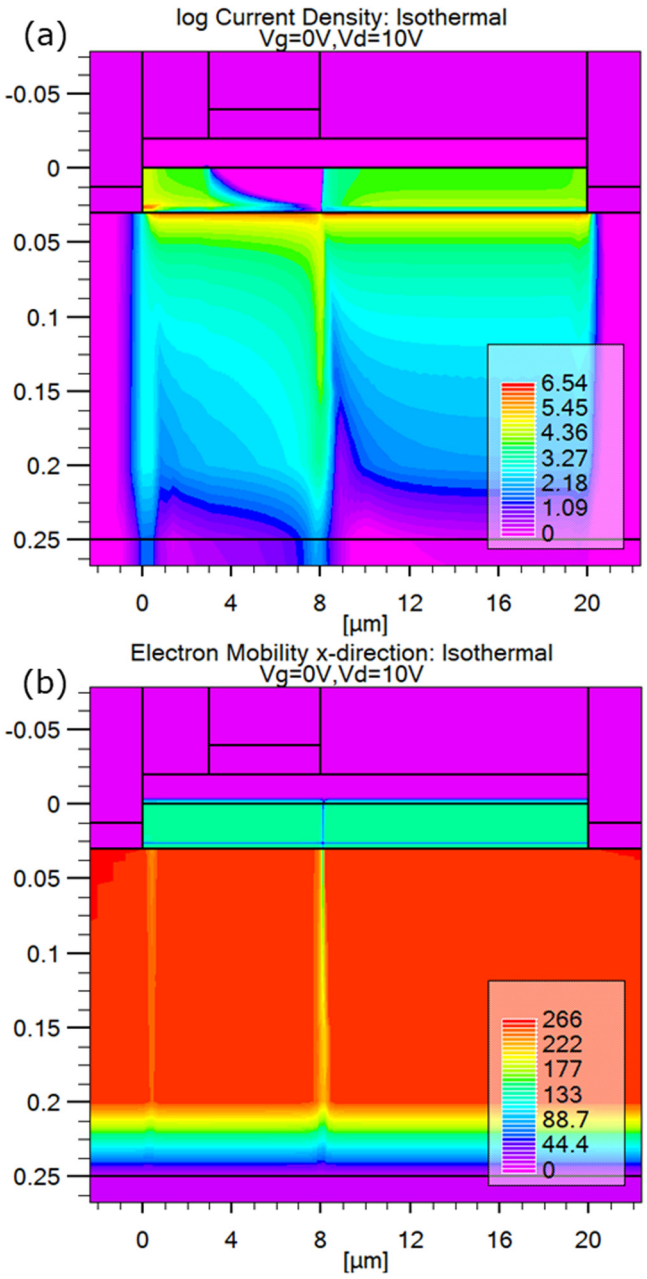

FIG. 5. Cross sections from an isothermal simulation at 300 °K for V_d at 10 V for (a) log current density (A/cm^2) and (b) x-component of electron mobility (cm^2/V s). As is common in transistors without field plates, there is a high electric field at the drain side of the gate edge, which results in (b) a local reduction in the x-component of electron mobility.

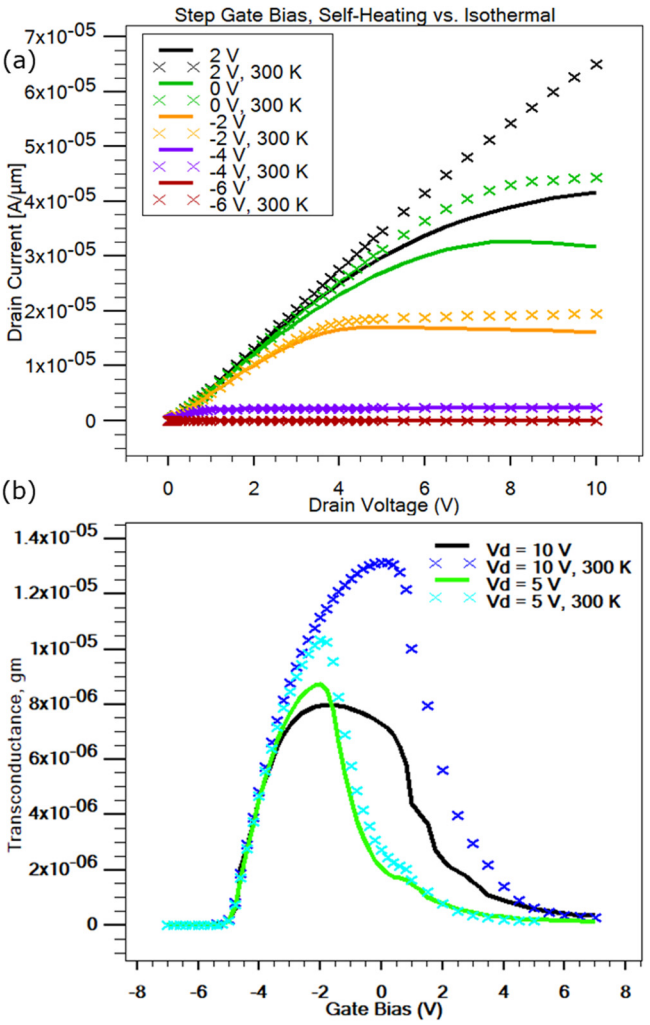

FIG. 6. Comparison of electrothermal simulation with self-heating vs isothermal simulation at 300 °K. (a) Drain current as a function of drain voltage for series of 2 V steps in gate voltage. (b) Transconductance as a function of gate bias at a drain voltage of 5 and 10 V. Current saturation due to the high-field mobility reduction effect and global heating mechanisms are inter-related. Still, a significant reduction is observed in drain current owing to the reduction in mobility due to self-heating compared to the isothermal simulation.

resistance, R_{th}, of 114 mm K°/W at 10 V (and 327 °K). The thermal resistance (Fig. 7) for the source metal thermal contact is 41% the thermal resistance for the bottom substrate thermal contact (Fig. 3).

A similar thermal resistance of the overall device is found in a simulation (not shown) for a device formed on a 20 μm substrate with a bottom thermal contact. This result is reasonable as the 20 μm distance to the substrate base is similar to the distance from the drain edge of the gate to the source contact. Hence, thinning the substrate is another approach; however, the propensity for β-Ga_2O_3 to cleave discourages a postgrowth wafer thinning approach. Still, several works have demonstrated devices processed on exfoliated Ga_2O_3 films with a thickness typically less than 10 μm.[10–13]

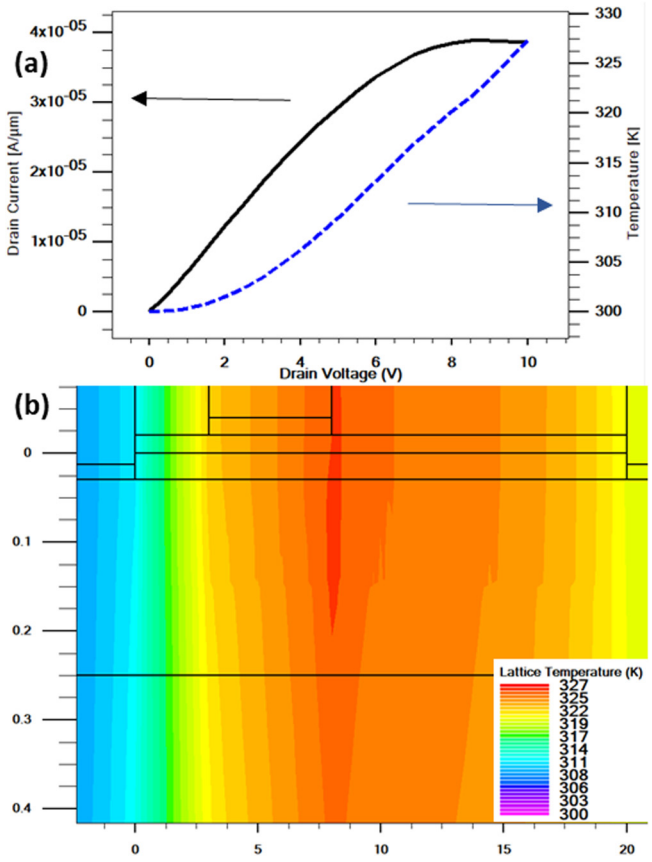

FIG. 7. Simulation with heat extraction via source metal. (a) Drain current and temperature as a function of drain voltage at zero gate bias. (b) Temperature (°K) cross sections for V_d at 10 V. The temperature vs drain bias in (a) displays a slope of 3.4 K°/V for V_d greater than 5 V.

IV. DISCUSSION

A. Self-heating and mobility

Thermal management is an important design consideration in all semiconductor power devices.[4,14] The simulations in this work show that self-heating owing to the low thermal conductivity of β-Ga_2O_3 dramatically lowers the mobility in the channel region, which increases the on-state resistance at moderate current densities. The low thermal conductivity of β-Ga_2O_3 necessitates advanced thermal management solutions for operation at even moderate power levels.[15,16] Candidate solutions include flip-chip designs where heat is extracted globally from the top surface as well as more nuanced modification of the gate region to enhance local heat extraction at or near the gate.[17–19] Naturally, thermal mapping of the device surface or depth directly measures the thermal response of the device.[20] Nevertheless, these measurements can be obscured by the contact structure. Additionally, a thermoreflectance imaging measurement is complicated by the requirement for illumination greater than the wide bandgap of β-Ga_2O_3. As outlined in this paper, understanding the relation of self-heating on the response of the drain current to applied gate bias and drain voltage provides an additional assessment of the thermal management in the device structure.

B. Modulation doping considerations of β-Ga_2O_3 modulation-doped field effect transistor

The presence of residual charge at the point of modulation doping is undesired as this creates a secondary channel that hampers the ability to modulate the primary channel. This charge at the modulation-doping point can be confirmed by an inflection in the transconductance curve. Specifically, as this charge is spatially closer to the gate metal, this inflection occurs at a more positive gate bias relative to the primary channel, which is deeper in the structure.

See the supplementary material[23] for design rules for the modulation-doped structure with a goal of maximizing the concentration of electrons in the potential well while minimizing the low-mobility secondary channel at the modulation-doped layer. An emphasis is placed on mitigating three limitations related to the deposition of β-Ga_2O_3, specifically, the inability to deposit high-quality β-$(Al_xGa_{1-x})_2O_3$ with an aluminum mole fraction greater than approximately 0.25, the difficulty to deposit a high concentration of dopant atoms without the formation of its native oxide, and the unintentional dopant atom exponential decay tail. Simulations for an aluminum mole fraction of 0.25 show that proper selection of the barrier thickness and modulation-doping level, including accounting for any asymmetric broadening, can yield a dense electron channel confined primarily to the potential well at the $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ interface.

V. SUMMARY AND CONCLUSIONS

The wide bandgap and related high critical breakdown field of β-Ga_2O_3 enables a high-voltage lateral transistor designed for low on-resistance as well as operation at high frequency, which reduces the size and weight of the passive circuit elements in the overall system.[21,22] In this work, an accurate approximation for mobility as a function of temperature and dopant concentration is presented and employed in an electrothermal simulation of an $(Al_xGa_{1-x})_2O_3/Ga_2O_3$ modulation-doped field effect transistor (MODFET). A decrease in drain current was attributed to a position-dependent mobility reduction caused by a coupled self-heating mechanism and a high electric-field mobility reduction mechanism. Thermal management is a key design issue in all power semiconductor devices. The low thermal conductivity of Ga_2O_3 hampers any design where heat must flow over any appreciable thickness of Ga_2O_3. A heatsink via the source contact is discussed and shown to reduce the temperature of the active device channel.

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should be inferred. The work at Korea University was supported by the Korea Institute of Energy Technology Evaluation and Planning (No. 20172010104830) and the National Research Foundation of Korea (No. 2020M3H4A3081799).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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